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PUB-NO: JP02001044156A
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TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE AND CHEMICAL POLISHING APPARATUS

PUBN-DATE: February 16, 2001

INVENTOR-INFORMATION:
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APPL-NO: JP11210782
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INT-CL (IPC): H01 L 21/304; B24 B 37/00; H01 L 21/28; H01 L 21/3205

ABSTRACT:

PROBLEM TO BE SOLVED: To improve LSI yield by improving the planarity of a semiconductor device for suppressing distribution of wiring sheet resistance, regardless of the density of a wiring pattern.

SOLUTION: An insulating film 12 of SiO2 or the like is formed on a substrate 11. Wiring grooves 13 having different pattern densities are made in the insulating film 12, and then a barrier metal layer 14 of TaN or the like and a wiring metal layer 15 of Cu or the like are deposited sequentially thereon. In order to form a wiring 16 in the wiring grooves 13, the wiring metal layer 15 and barrier metal layer 14 are polished sequentially by a chemical mechanical polishing(CMP) apparatus. When polishing reaches the overpolished level, polishing is carried out with use of a slurry containing polishing abrasive grains of silica, alumina or the like and with an adjusted pH level which is not smaller than 5 and not larger than 13, so that the value of the polishing rate ratio between the film 15 and 12 is 0.2-5, whereby erosion is suppressed and the wiring layer 16 is made flush with the insulating film 12 within the wiring grooves 13.

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